This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1 – 80 (canceled)

Claim 81 (previously presented)

A memory, comprising:

a plurality of memory cells:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus for delivering said supply voltages; and

a package encapsulating said memory, said package including a lead frame forming a part of said power distribution bus.

Claim 82 (canceled)

A method of encapsulating a solid state device of the type having a lead frame connected to the bonding pads of the device, wherein the improvement comprises utilizing tie bars to provide support to the lead fingers during the encapsulation process.

Claim 83 (canceled)

The method of claim 82 wherein a portion of said lead frame forms part of the electrical circuit of the solid state device.

Claim 84 (canceled)

A method of placing a solid state device into a test mode comprising:

placing a supervoltage test mode signal on a pin of the solid state device;

applying a test key to certain pins of the solid state device; and

placing a second supervoltage test mode signal on said pin to read the test key.

Claim 85 (previously presented)

The memory of claim 81 wherein said plurality of memory cells is organized into a plurality of individual arrays, said individual arrays organized into rows and columns to form

a plurality of array blocks, said power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks.

Claim 86 (previously presented)

The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

Claim 87 (previously presented)

The memory of claim 86 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the array blocks.

Claim 88 (previously presented)

The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

Claim 89 (previously presented)

The memory of claim 88 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the array blocks.

Claim 90 (previously presented)

The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

Claim 91 (previously presented)

The memory of claim 90 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the array blocks.

Claim 92 (previously presented)

The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage, and wherein said certain of said first and second pluralities of conductors for carrying a ground voltage are connected to said lead frame .

Claim 93 (previously presented)

The memory of claim 92 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the array blocks.

Claim 94 (previously presented)

The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

Claim 95 (previously presented)

The memory of claim 94 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the array blocks.

Claim 96 (previously presented)

The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

Claim 97 (previously presented)

The memory of claim 96 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the array blocks.

Claim 98 (previously presented)

The memory of claim 85 wherein certain of said first plurality of conductors are for carrying a peripheral voltage.

Claim 99 (previously presented)

The memory of claim 98 additionally comprising a plurality of switches each controlling the distribution of the peripheral voltage to one of the array blocks.

Claim 100 (previously presented)

The memory of claim 85 wherein said first plurality of conductors extend from an area located centrally with respect to the memory blocks.

Claim 101 (previously presented)

The memory of claim 85 additionally comprising a third plurality of conductors running parallel to a plurality of input/output pads for receiving external power from the pads

and for supplying the external power to a plurality of voltage supplies located proximate to the pads.

Claim 102 (previously presented)

The memory of claim 85 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 103 (previously presented)

The memory of claim 102 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 104 (previously presented)

A memory, comprising:

a plurality of memory cells, said plurality of memory cells organized into a plurality of individual arrays, said individual arrays organized into rows and columns to form a plurality of array blocks,:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks; and

a package encapsulating said memory, said package including a lead frame forming a ground bus.

Claim 105 (previously presented)

The memory of claim 104 wherein said array blocks include datalines running between adjacent columns of individual arrays and I/O lines running perpendicularly to said

datalines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals between said I/O lines and said datalines.

Claim 106 (previously presented)

The memory of claim 105 wherein said multiplexers are positioned at every second individual array.

Claim 107 (previously presented)

The memory of claim 104 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 108 (previously presented)

The memory of claim 107 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 109 (previously presented)

The memory of claim 107 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 110 (previously presented)

The memory of claim 109 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 111 (previously presented)

The memory of claim 104 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external

voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 112 (previously presented)

The memory of claim 104 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 113 (previously presented)

The memory of claim 112 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 114 (previously presented)

The memory of claim 112 wherein said plurality of power amplifiers are divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 115 (previously presented)

The memory of claim 104 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 116 (previously presented)

The memory of claim 115 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 117 (previously presented)

The memory of claim 104 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 118 (previously presented)

The memory of claim 104 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 119 (previously presented)

The memory of claim 104 wherein said memory provides at least 256 meg of storage.

Claim 120 (previously presented)

The memory of claim 119 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 121 (previously presented)

The memory of claim 104 wherein said plurality of pads and said plurality of voltage supplies are centrally located with respect to said plurality of array blocks.

Claim 122 (previously presented)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

a plurality of memory cells:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus for delivering said supply voltages; and

a package encapsulating said memory, said package including a lead frame forming a part of said power distribution bus.

Claim 123 (previously presented)

The system of claim 122 wherein said plurality of memory cells is organized into a plurality of individual arrays, said individual arrays organized into rows and columns to form a plurality of array blocks, said power distribution bus comprised of a first plurality of

conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks.

Claim 124 (previously presented)

The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

Claim 125 (previously presented)

The system of claim 124 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the array blocks.

Claim 126 (previously presented)

The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

Claim 127 (previously presented)

The system of claim 126 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the array blocks.

Claim 128 (previously presented)

The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

Claim 129 (previously presented)

The system of claim 128 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the array blocks.

Claim 130 (previously presented)

The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage, and wherein said certain of said first and second pluralities of conductors for carrying a ground voltage are connected to said lead frame .

Claim 131 (previously presented)

The system of claim 130 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the array blocks.

Claim 132 (previously presented)

The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

Claim 133 (previously presented)

The system of claim 132 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the array blocks.

Claim 134 (previously presented)

The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

Claim 135 (previously presented)

The system of claim 134 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the array blocks.

Claim 136 (previously presented)

The system of claim 123 wherein certain of said first plurality of conductors are for carrying a peripheral voltage.

Claim 137 (previously presented)

The system of claim 136 additionally comprising a plurality of switches each controlling the distribution of the peripheral voltage to one of the array blocks.

Claim 138 (previously presented)

The system of claim 123 wherein said first plurality of conductors extend from an area located centrally with respect to the memory blocks.

Claim 139 (previously presented)

The system of claim 123 additionally comprising a third plurality of conductors running parallel to a plurality of input/output pads for receiving external power from the pads

and for supplying the external power to a plurality of voltage supplies located proximate to the pads.

Claim 140 (previously presented)

The system of claim 123 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 141 (previously presented)

The system of claim 140 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 142 (previously presented)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

a plurality of memory cells, said plurality of memory cells organized into a plurality of individual arrays, said individual arrays organized into rows and columns to for a plurality of array blocks;

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks; and

a package encapsulating said memory, said package including a lead frame forming a ground bus.

Claim 143 (previously presented)

The system of claim 142 wherein said array blocks include datalines running between adjacent columns of individual arrays and I/O lines running perpendicularly to said datalines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals between said I/O lines and said datalines.

Claim 144 (previously presented)

The system of claim 143 wherein said multiplexers are positioned at every second individual array.

Claim 145 (previously presented)

The system of claim 142 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 146 (previously presented)

The system of claim 145 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 147 (previously presented)

The system of claim 145 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 148 (previously presented)

The system of claim 147 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 149 (previously presented)

The system of claim 142 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 150 (previously presented)

The system claim 142 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 151 (previously presented)

The system of claim 150 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 152 (previously presented)

The system of claim 150 wherein said plurality of power amplifiers are divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 153 (previously presented)

The system of claim 142 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 154 (previously presented)

The system of claim 153 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 155 (previously presented)

The system of claim 142 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 156 (previously presented)

The system of claim 142 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 157 (previously presented)

The system of claim 142 wherein said memory provides at least 256 meg of storage.

Claim 158 (previously presented)

The system of claim 157 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 159 (previously presented)

The system of claim 142 wherein said plurality of pads and said plurality of voltage supplies are centrally located with respect to said plurality of array blocks.